Compact, Precision Six Degrees of Freedom Inertial Sensor

Data Sheet

ADIS16445

FEATURES

Triaxial digital gyroscope with digital range scaling
±62°/sec, ±125°/sec, ±250°/sec settings
Axis-to-axis alignment, <0.05°
Triaxial digital accelerometer, ±5 *g* minimum
Autonomous operation and data collection
No external configuration commands required
175 ms start-up time
Factory calibrated sensitivity, bias, and axial alignment
Calibration temperature range: −40°C to +70°C
SPI-compatible serial interface
Embedded temperature sensor
Programmable operation and control
Automatic and manual bias correction controls
Bartlett window FIR length, number of taps
Digital I/O: data ready, alarm indicator, general-purpose
Alarms for condition monitoring
Enable external sample clock input up to 1.1 kHz
Single command self test
Single-supply operation: 3.15 V to 3.45 V
2000 *g* shock survivability
Operating temperature range: −40°C to +85°C

APPLICATIONS

Platform stabilization and control
Navigation
Robotics

GENERAL DESCRIPTION

The ADIS16445 *i*Sensor® device is a complete inertial system that includes a triaxial gyroscope and a triaxial accelerometer. Each sensor in the ADIS16445 combines industry-leading *i*MEMS® technology with signal conditioning that optimizes dynamic performance. The factory calibration characterizes each sensor for sensitivity, bias, alignment, and linear acceleration (gyroscope bias). As a result, each sensor has its own dynamic compensation formulas that provide accurate sensor measurements.

The ADIS16445 provides a simple, cost-effective method for integrating accurate, multiaxis inertial sensing into industrial systems, especially when compared with the complexity and investment associated with discrete designs. All necessary motion testing and calibration are part of the production process at the factory, greatly reducing system integration time. Tight orthogonal alignment simplifies inertial frame alignment in navigation systems. The SPI and register structures provide a simple interface for data collection and configuration control.

The ADIS16445 has a compatible pinout for systems that currently use other Analog Devices, Inc., IMU products (ADIS163xx/ADIS164xx). The ADIS16445 is packaged in a module that is approximately 24.1 mm × 37.7 mm × 10.8 mm and has a standard connector interface.

FUNCTIONAL BLOCK DIAGRAM

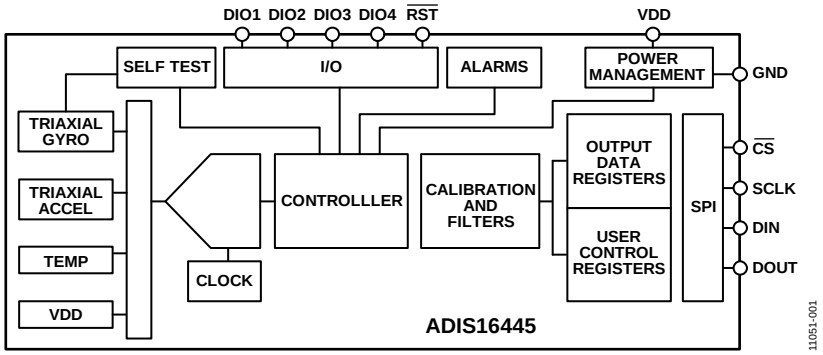

Figure 1.

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REVISION HISTORY

10/12—Revision 0: Initial Version

SPECIFICATIONS

T_A = 25°C, VDD = 3.3 V, angular rate = 0°/sec, dynamic range = ±250°/sec ± 1 *g*, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
GYROSCOPES					
Dynamic Range		±250			°/sec
Initial Sensitivity	±250°/sec, see Table 12	0.0099	0.01	0.0101	°/sec/LSB
	±125°/sec		0.005		°/sec/LSB
	±62°/sec		0.0025		°/sec/LSB
Sensitivity Temperature Coefficient	−40°C ≤ T_A ≤ +70°C		±40		ppm/°C
Misalignment	Axis to axis		±0.05		Degrees
	Axis to frame (package)		±0.5		Degrees
Nonlinearity	Best fit straight line		±0.1		% of FS
Initial Bias Error			0.5		°/sec
In-Run Bias Stability	1 σ, SMPL_PRD = 0x0001		12		°/hr
Angular Random Walk	1 σ, SMPL_PRD = 0x0001		0.56		°/√hr
Bias Temperature Coefficient	−40°C ≤ T_A ≤ +85°C		±0.005		°/sec/°C
Linear Acceleration Effect on Bias	Any axis, 1 σ (MSC_CTRL[6] = 1)		±0.015		°/sec/*g*
Bias Supply Sensitivity	+3.15 V ≤ VDD ≤ +3.45 V		±0.2		°/sec/V
Output Noise	±250°/sec range, no filtering		0.22		°/sec rms
Rate Noise Density	f = 25 Hz, ±250°/sec range, no filtering		0.011		°/sec/√Hz rms
−3 dB Bandwidth			330		Hz
Sensor Resonant Frequency			17.5		kHz
ACCELEROMETERS	Each axis				
Dynamic Range		±5			*g*
Initial Sensitivity	See Table 16 for data format	0.2475	0.25	0.2525	m*g*/LSB
Sensitivity Temperature Coefficient	−40°C ≤ T_A ≤ +70°C		±40		ppm/°C
Misalignment	Axis to axis		±0.2		Degrees
	Axis to frame (package)		±0.5		Degrees
Nonlinearity	Best fit straight line		±0.2		% of FS
Initial Bias Error			±8		m*g*
In-Run Bias Stability	1 σ, SMPL_PRD = 0x0001		0.075		m*g*
Velocity Random Walk	1 σ, SMPL_PRD = 0x0001		0.073		m/sec/√hr
Bias Temperature Coefficient	−40°C ≤ T_A ≤ +85°C		±0.04		m*g*/°C
Bias Supply Sensitivity	+3.15 V ≤ VDD ≤ +3.45 V		1.5		m*g*/V
Output Noise	No filtering		2.25		m*g* rms
Noise Density	No filtering		0.105		m*g*/√Hz rms
−3 dB Bandwidth			330		Hz
Sensor Resonant Frequency			5.5		kHz
TEMPERATURE					
Sensitivity	See Table 17		0.07386		°C/LSB
LOGIC INPUTS[1]					
Input High Voltage, V_{IH}		2.0			V
Input Low Voltage, V_{IL}				0.8	V
Logic 1 Input Current, I_{IH}	V_{IH} = 3.3 V		±0.2	±10	µA
Logic 0 Input Current, I_{IL}	V_{IL} = 0 V				
All Pins Except $\overline{RST}$			40	60	µA
$\overline{RST}$ Pin			1		mA
Input Capacitance, C_{IN}			10		pF

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DIGITAL OUTPUTS[1]					
Output High Voltage, V_{OH}	I_{SOURCE} = 1.6 mA	2.4			V
Output Low Voltage, V_{OL}	I_{SINK} = 1.6 mA			0.4	V
FLASH MEMORY	Endurance[2]	10,000			Cycles
Data Retention[3]	T_J = 85°C	20			Years
FUNCTIONAL TIMES[4]	Time until new data is available				
Power-On Start-Up Time			175		ms
Reset Recovery Time			55		ms
Flash Memory Back-Up Time			55		ms
Flash Memory Test Time			20		ms
Automatic Self-Test Time	SMPL_PRD = 0x0001		16		ms
CONVERSION RATE					
xGYRO_OUT, xACCL_OUT	SMPL_PRD = 0x0001		819.2		SPS
Clock Accuracy				±3	%
Sync Input Clock[5]		0.8		1.1	kHz
POWER SUPPLY	Operating voltage range, VDD	3.15	3.3	3.45	V
Power Supply Current	VDD = 3.15 V		74		mA

[1] The digital I/O signals are driven by an internal 3.3 V supply, and the inputs are 5 V tolerant.
[2] Endurance is qualified as per JEDEC Standard 22, Method A117, and measured at −40°C, +25°C, +85°C, and +125°C.
[3] The data retention lifetime equivalent is at a junction temperature (T_J) of 85°C as per JEDEC Standard 22, Method A117. Data retention lifetime decreases with junction temperature.
[4] These times do not include thermal settling and internal filter response times (330 Hz bandwidth), which may affect overall accuracy.
[5] The sync input clock functions below the specified minimum value but at reduced performance levels.

TIMING SPECIFICATIONS

T_A = 25°C, VDD = +3.3 V, unless otherwise noted.

Table 2.

		Normal Mode			Burst Read			
Parameter	**Description**	**Min[1]**	**Typ**	**Max**	**Min[1]**	**Typ**	**Max**	**Unit**
f_{SCLK}	Serial clock	0.01		2.0	0.01		1.0	MHz
t_{STALL}	Stall period between data	9			N/A[2]			µs
$t_{READRATE}$	Read rate	40						µs
$t_{\overline{CS}}$	Chip select to SCLK edge	48.8			48.8			ns
t_{DAV}	DOUT valid after SCLK edge			100			100	ns
t_{DSU}	DIN setup time before SCLK rising edge	24.4			24.4			ns
t_{DHD}	DIN hold time after SCLK rising edge	48.8			48.8			ns
t_{SCLKR}, t_{SCLKF}	SCLK rise/fall times, not shown in timing diagrams		5	12.5		5	12.5	ns
t_{DR}, t_{DF}	DOUT rise/fall times, not shown in timing diagrams		5	12.5		5	12.5	ns
t_{SFS}	$\overline{CS}$ high after SCLK edge	5			5			ns
t_1	Input sync positive pulse width	25			25			µs
t_{STDR}	Input sync to data ready valid transition		670			670		µs
t_{NV}	Data invalid time		210			210		µs
t_3	Input sync period	910			910			µs

[1] Guaranteed by design and characterization, but not tested in production.
[2] When using the burst read mode, the stall period is not applicable.

Timing Diagrams

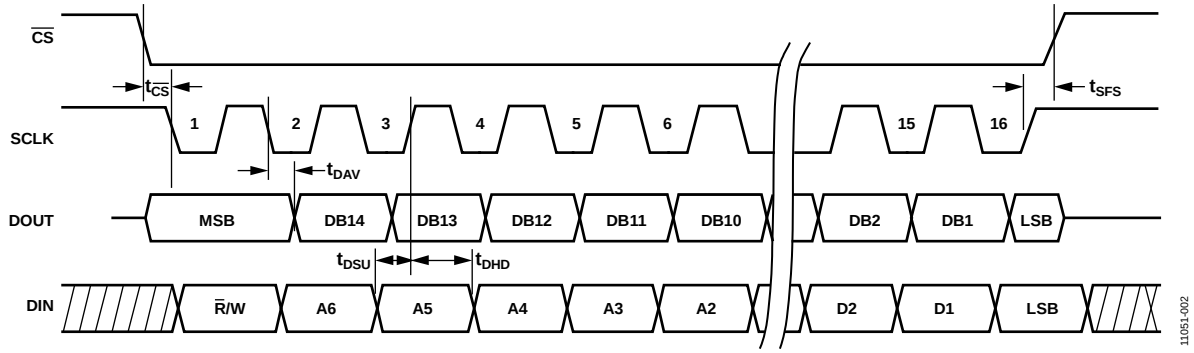


Figure 2. SPI Timing and Sequence

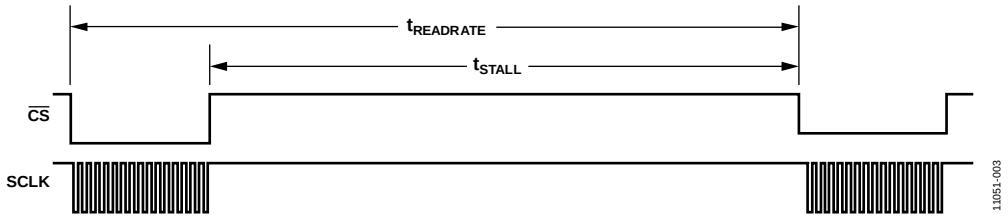


Figure 3. Stall Time and Data Rate

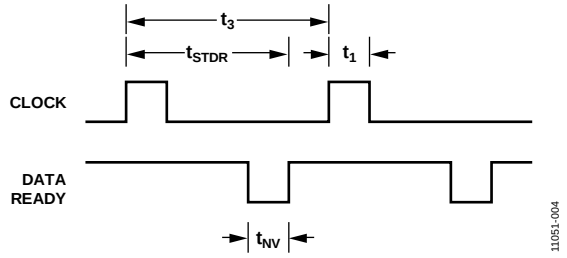


Figure 4. Input Clock Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Acceleration	
Any Axis, Unpowered	2000 *g*
Any Axis, Powered	2000 *g*
VDD to GND	−0.3 V to +3.45 V
Digital Input Voltage to GND	−0.3 V to +VDD + 0.3 V
Digital Output Voltage to GND	−0.3 V to +VDD + 0.3 V
Temperature	
Operating Range	−40°C to +85°C
Storage Range	−65°C to +125°C[1, 2]

[1] Extended exposure to temperatures outside the specified temperature range of −40°C to +105°C can adversely affect the accuracy of the factory calibration. For best accuracy, store the parts within the specified operating range of −40°C to +105°C.

[2] Although the device is capable of withstanding short-term exposure to 150°C, long-term exposure threatens internal mechanical integrity.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

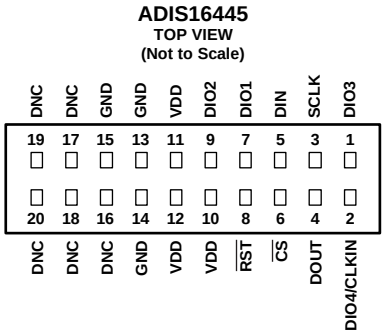
Table 4. Package Characteristics

Package Type	θ_{JA} (°C/W)	θ_{JC} (°C/W)	Mass (grams)
20-Lead Module (ML-20-3)	36.5	16.9	15

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

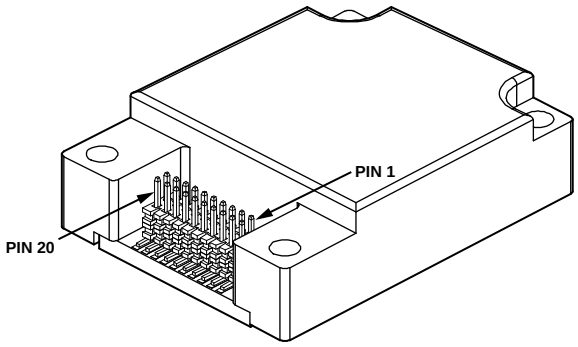
PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. THIS REPRESENTATION DISPLAYS THE TOP VIEW WHEN THE CONNECTOR IS VISIBLE AND FACING UP.
2. MATING CONNECTOR: SAMTEC CLM-110-02 OR EQUIVALENT.
3. DNC = DO NOT CONNECT.

11051-005

Figure 5. Pin Configuration



11051-006

Figure 6. Pin Locations

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1	DIO3	I/O	Configurable Digital Input/Output.
2	DIO4/CLKIN	I/O	Configurable Digital Input/Output or Sync Clock Input.
3	SCLK	I	SPI Serial Clock.
4	DOUT	O	SPI Data Output. Clocks the output on the SCLK falling edge.
5	DIN	I	SPI Data Input. Clocks the input on the SCLK rising edge.
6	$\overline{CS}$	I	SPI Chip Select.
7	DIO1	I/O	Configurable Digital Input/Output.
8	$\overline{RST}$	I	Reset.
9	DIO2	I/O	Configurable Digital Input/Output.
10, 11, 12	VDD	S	Power Supply.
13, 14, 15	GND	S	Power Ground.
16, 17, 18, 19, 20	DNC	N/A	Do Not Connect. Do not connect to these pins.

[1] S is supply, O is output, I is input, N/A is not applicable.

TYPICAL PERFORMANCE CHARACTERISTICS

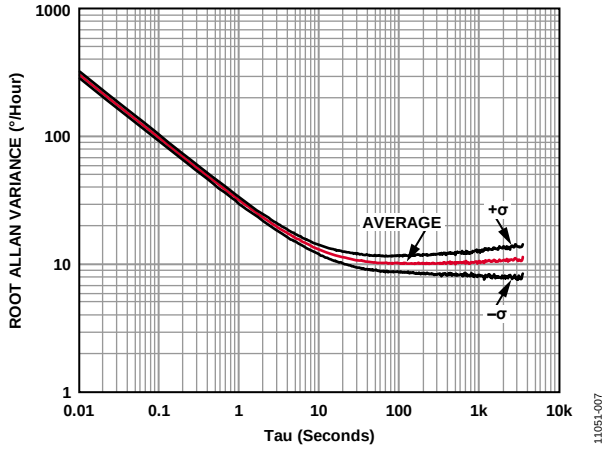


Figure 7. Gyroscope Root Allan Variance

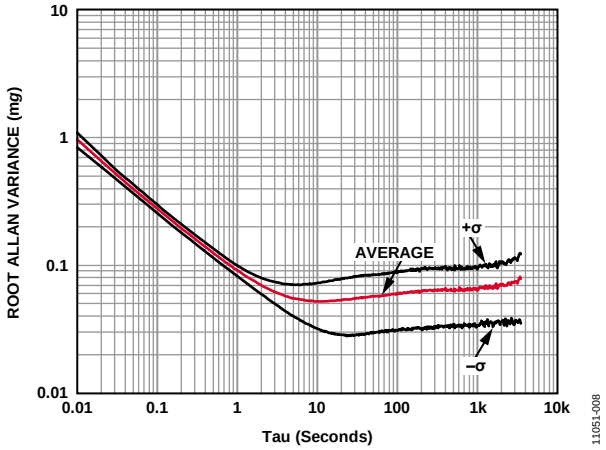


Figure 8. Accelerometer Root Allan Variance

USER REGISTERS

Table 6. User Register Memory Map

Name	R/W	Flash Backup	Address[1]	Default	Function	Bit Assignments
FLASH_CNT	R	Yes	0x00	N/A	Flash memory write count	See Table 26
Reserved	N/A	N/A	0x02	N/A	N/A	N/A
XGYRO_OUT	R	No	0x04	N/A	X-axis gyroscope output	See Table 9
YGYRO_OUT	R	No	0x06	N/A	Y-axis gyroscope output	See Table 10
ZGYRO_OUT	R	No	0x08	N/A	Z-axis gyroscope output	See Table 11
XACCL_OUT	R	No	0x0A	N/A	X-axis accelerometer output	See Table 13
YACCL_OUT	R	No	0x0C	N/A	Y-axis accelerometer output	See Table 14
ZACCL_OUT	R	No	0x0E	N/A	Z-axis accelerometer output	See Table 15
Reserved	N/A	N/A	0x10 to 0x16	N/A	Reserved	N/A
TEMP_OUT	R	No	0x18	N/A	Temperature output	See Table 17
XGYRO_OFF	R/W	Yes	0x1A	0x0000	X-axis gyroscope bias offset factor	See Table 30
YGYRO_OFF	R/W	Yes	0x1C	0x0000	Y-axis gyroscope bias offset factor	See Table 31
ZGYRO_OFF	R/W	Yes	0x1E	0x0000	Z-axis gyroscope bias offset factor	See Table 32
XACCL_OFF	R/W	Yes	0x20	0x0000	X-axis acceleration bias offset factor	See Table 33
YACCL_OFF	R/W	Yes	0x22	0x0000	Y-axis acceleration bias offset factor	See Table 34
ZACCL_OFF	R/W	Yes	0x24	0x0000	Z-axis acceleration bias offset factor	See Table 35
Reserved	N/A	N/A	0x26 to 0x30	N/A	Reserved	N/A
GPIO_CTRL	R/W	No	0x32	0x0000	Auxiliary digital input/output control	See Table 27
MSC_CTRL	R/W	Yes	0x34	0x0006	Miscellaneous control	See Table 24
SMPL_PRD	R/W	Yes	0x36	0x0001	Internal sample period (rate) control	See Table 28
SENS_AVG	R/W	Yes	0x38	0x0402	Dynamic range and digital filter control	See Table 29
Reserved	N/A	N/A	0x3A	N/A	Reserved	N/A
DIAG_STAT	R	No	0x3C	0x0000	System status	See Table 25
Reserved	N/A	N/A	0x3A	N/A	Reserved	N/A
GLOB_CMD	W	N/A	0x3E	0x0000	System command	See Table 19
ALM_MAG1	R/W	Yes	0x40	0x0000	Alarm 1 amplitude threshold	See Table 36
ALM_MAG2	R/W	Yes	0x42	0x0000	Alarm 2 amplitude threshold	See Table 37
ALM_SMPL1	R/W	Yes	0x44	0x0000	Alarm 1 sample size	See Table 38
ALM_SMPL2	R/W	Yes	0x46	0x0000	Alarm 2 sample size	See Table 39
ALM_CTRL	R/W	Yes	0x48	0x0000	Alarm control	See Table 40
Reserved	N/A	N/A	0x4A to 0x51	N/A	Reserved	N/A
LOT_ID1	R	Yes	0x52	N/A	Lot identification number	See Table 20
LOT_ID2	R	Yes	0x54	N/A	Lot identification number	See Table 21
PROD_ID	R	Yes	0x56	0x403D	Product identifier	See Table 22
SERIAL_NUM	R	Yes	0x58	N/A	Lot-specific serial number	See Table 23

[1] Each register contains two bytes. The address of the lower byte is displayed. The address of the upper byte is equal to the address of the lower byte plus 1.

USER INTERFACE

The ADIS16445 is an autonomous system that requires no user initialization. When it has a valid power supply, it initializes itself and starts sampling, processing, and loading sensor data into the output registers at a sample rate of 819.2 SPS. DIO1 pulses high after each sample cycle concludes. The SPI interface enables simple integration with many embedded processor platforms, as shown in Figure 9 (electrical connection) and Table 7 (pin functions).

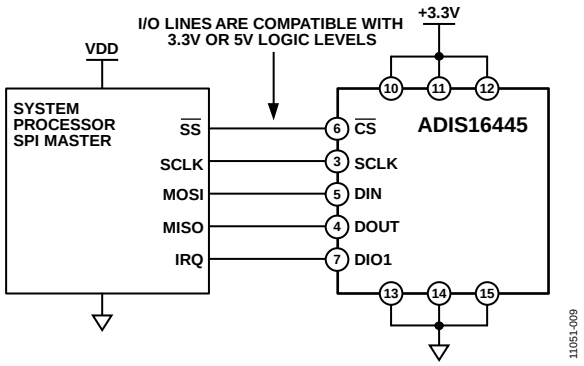


Figure 9. Electrical Connection Diagram

Table 7. Generic Master Processor Pin Names and Functions

Pin Name	Function
$\overline{SS}$	Slave select
SCLK	Serial clock
MOSI	Master output, slave input
MISO	Master input, slave output
IRQ	Interrupt request

The ADIS16445 SPI interface supports full duplex serial communication (simultaneous transmit and receive) and uses the bit sequence shown in Figure 12. Table 8 provides a list of the most common settings that require attention to initialize the serial port of a processor for the ADIS16445 SPI interface.

Table 8. Generic Master Processor SPI Settings

Processor Setting	Description
Master	The ADIS16445 operates as a slave
SCLK ≤ 2 MHz[1]	Maximum serial clock rate
SPI Mode 3	CPOL = 1 (polarity), CPHA = 1 (phase)
MSB-First Mode	Bit sequence
16-Bit Mode	Shift register/data length

[1] For burst read, SCLK rate ≤ 1 MHz.

READING SENSOR DATA

The ADIS16445 provides two different options for acquiring sensor data: a single register and a burst register. A single register read requires two 16-bit SPI cycles. The first cycle requests the contents of a register using the bit assignments in Figure 12. Bit DC7 to Bit DC0 are don't cares for a read, and then the output register contents follow on DOUT during the second sequence. Figure 10 includes three single register reads in succession.

In this example, the process starts with DIN = 0x0400 to request the contents of XGYRO_OUT, then follows with 0x0600 to request YGYRO_OUT, and 0x0800 to request ZGYRO_OUT. Full duplex operation enables processors to use the same 16-bit SPI cycle to read data from DOUT while requesting the next set of data on DIN. Figure 11 provides an example of the four SPI signals when reading XGYRO_OUT in a repeating pattern.

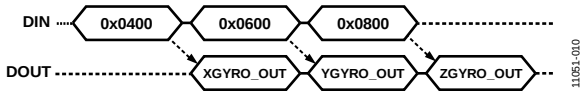


Figure 10. SPI Read Example

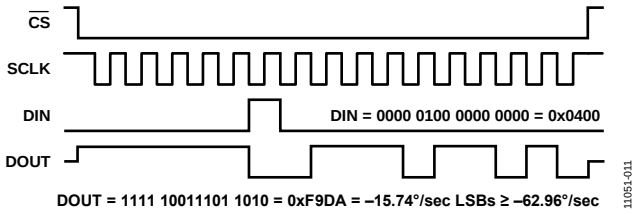


Figure 11. Example SPI Read, Second Sequence, SENS_AVG[15:8] = 0x04

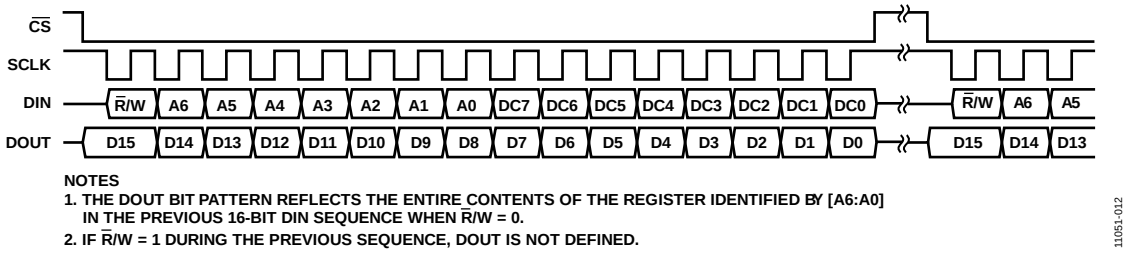


Figure 12. SPI Communication Bit Sequence

Burst Read Function

The burst read function enables the user to read all output registers using one command on the DIN line, 0x3E00. When using this mode, one can read all of the data in one continuous stream of bits (no stall time between each register). After the 0x3E00 command, use 12 sequential, 16-bit read commands to complete the sequence (DIN is "don't care" after 0x3E00). Figure 13 provides the burst read sequence of data on each SPI signal. The sequence starts with writing 0x3E00 to DIN, followed by each output register clocking out on DOUT, in the order in which they appear in Figure 12.

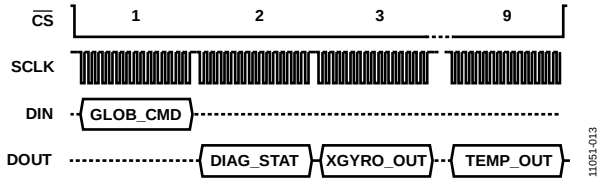


Figure 13. Burst Read Sequence

SPI Read Test Sequence

Figure 14 provides a test pattern for testing the SPI communication. In this pattern, write 0x5600 to the DIN line in a repeating pattern and raise chip select for at least 9 µs between each 16-bit sequence. Starting with the second 16-bit sequence, DOUT produces the contents of the PROD_ID register, 0x403D (see Table 22).

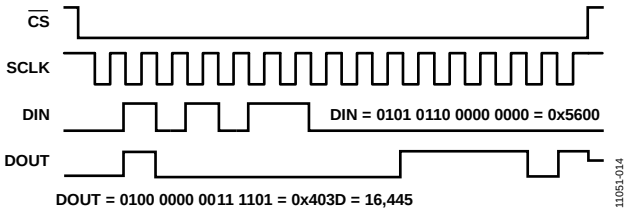


Figure 14. SPI Test Read Pattern DIN = 0x5600, DOUT = 0x403D

DEVICE CONFIGURATION

The control registers in Table 6 provide users with a variety of configuration options. The SPI provides access to these registers, one byte at a time, using the bit assignments in Figure 12. Each register has 16 bits, where Bits[7:0] represent the lower address, and Bits[15:8] represent the upper address. Figure 15 provides an example of writing 0x04 to Address 0x37 (SMPL_PRD[15:8], using DIN = 0xB704). This example reduces the sample rate by a factor of eight (see Table 28).

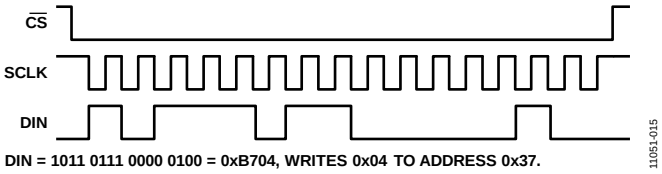


Figure 15. Example SPI Write Sequence

Dual Memory Structure

Writing configuration data to a control register updates its SRAM contents, which are volatile. After optimizing each relevant control register setting in a system, set GLOB_CMD[3] = 1 (DIN = 0xBE08) to back up these settings in nonvolatile flash memory. The flash backup process requires a valid power supply level for the entire process time, 75 ms. Table 6 provides a user register memory map that includes a flash backup column. A Yes in this column indicates that a register has a mirror location in flash and, when backed up properly, it automatically restores itself during startup or after a reset. Figure 16 provides a diagram of the dual memory structure used to manage operation and store critical user settings.

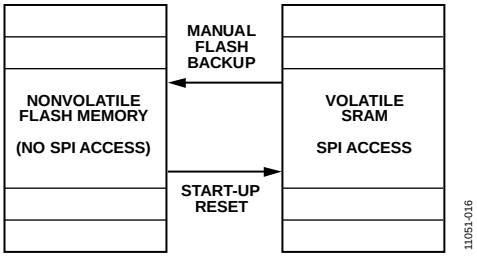


Figure 16. SRAM and Flash Memory Diagram

OUTPUT DATA REGISTERS

Each sensor in the ADIS16445 has a dedicated output register in the user register map (see Table 6). Figure 17 provides arrows, which describe the direction or rotation (g_X, g_Y, g_Z) and acceleration (a_X, a_Y, a_Z) that produces a positive response in the output data.

GYROSCOPES

XGYRO_OUT (see Table 9) contains x-axis gyroscope data (g_X in Figure 17), YGYRO_OUT (see Table 10) contains y-axis gyroscope data (g_Y in Figure 17), and ZGYRO_OUT (see Table 11) contains z-axis gyroscope data (g_Z in Figure 17). Table 12 illustrates the gyroscope data format with numerical examples.

Table 9. XGYRO_OUT (Base Address = 0x04), Read Only

Bits	Description
[15:0]	X-axis gyroscope data, twos complement format, 100 LSB/°/sec (SENS_AVG[15:8] = 0x04), 0°/sec = 0x0000

Table 10. YGYRO_OUT (Base Address = 0x06), Read Only

Bits	Description
[15:0]	Y-axis gyroscope data, twos complement format, 100 LSB/°/sec (SENS_AVG[15:8] = 0x04), 0°/sec = 0x0000

Table 11. ZGYRO_OUT (Base Address = 0x08), Read Only

Bits	Description
[15:0]	Z-axis gyroscope data, twos complement format, 100 LSB/°/sec (SENS_AVG[15:8] = 0x04), 0°/sec = 0x0000

Table 12. Rotation Rate, Twos Complement Format[1]

Rotation Rate (°/sec)	Decimal	Hex	Binary
+250	25,000	0x61A8	0110 0001 1010 1000
+2 ÷ 100	+2	0x0002	0000 0000 0000 0010
+1 ÷ 100	+1	0x0001	0000 0000 0000 0001
0	0	0x0000	0000 0000 0000 0000
−1 ÷ 100	−1	0xFFFF	1111 1111 1111 1111
−2 ÷ 100	−2	0xFFFE	1111 1111 1111 1110
−250	−25,000	0x9E58	1001 1110 0101 1000

[1] SENS_AVG[15:8] = 0x04, see Table 29.

ACCELEROMETERS

XACCL_OUT (see Table 13) contains x-axis accelerometer data (a_X in Figure 17), YACCL_OUT (see Table 14) contains y-axis accelerometer data (a_Y in Figure 17), and ZACCL_OUT (see Table 15) contains z-axis accelerometer data (a_Z in Figure 17). Table 16 illustrates the accelerometer data format with numerical examples.

Table 13. XACCL_OUT (Base Address = 0x0A), Read Only

Bits	Description
[15:0]	X-axis acceleration data, twos complement format, 4000 LSB/*g*, 0 *g* = 0x0000

Table 14. YACCL_OUT (Base Address = 0x0C), Read Only

Bits	Description
[15:0]	Y-axis acceleration data, twos complement format, 4000 LSB/*g*, 0 *g* = 0x0000

Table 15. ZACCL_OUT (Base Address = 0x0E), Read Only

Bits	Description
[15:0]	Z-axis acceleration data, twos complement format, 4000 LSB/*g*, 0 *g* = 0x0000

Table 16. Acceleration, Twos Complement Format

Acceleration (*g*)	Decimal	Hex	Binary
+5	20,000	0x4E20	0100 1110 0010 0000
+2 ÷ 4000	+2	0x0002	0000 0000 0000 0010
+1 ÷ 4000	+1	0x0001	0000 0000 0000 0001
0	0	0x0000	0000 0000 0000 0000
−1 ÷ 4000	−1	0xFFFF	1111 1111 1111 1111
−2 ÷ 4000	−2	0xFFFE	1111 1111 1111 1110
−5	−20,000	0xB1E0	1011 0001 1110 0000

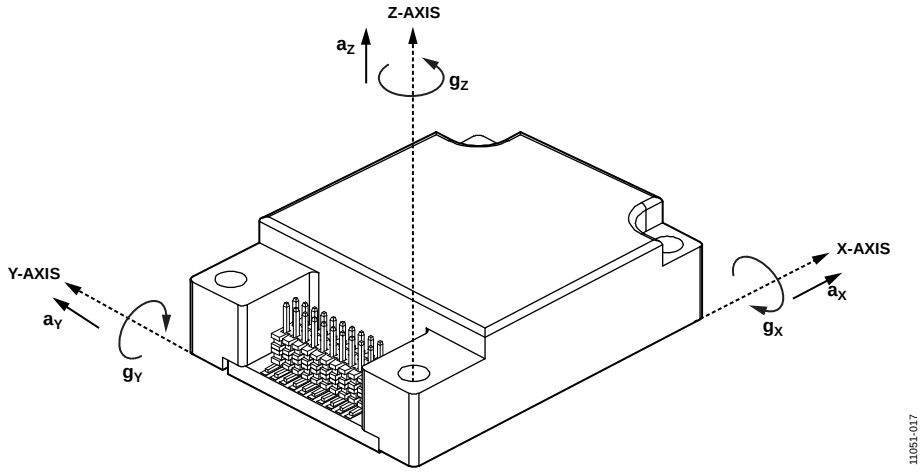


Figure 17. Inertial Sensor Direction Reference

INTERNAL TEMPERATURE

The internal temperature measurement data loads into the TEMP_OUT (see Table 17) register. Table 18 illustrates the temperature data format. Note that this temperature represents an internal temperature reading, which does not precisely represent external conditions. The intended use of TEMP_OUT is to monitor relative changes in temperature.

Table 17. TEMP_OUT (Base Address = 0x18), Read Only

Bits	Description
[15:12]	Not used
[11:0]	Twos complement, 0.07386°C/LSB, 31°C = 0x000

Table 18. Temperature, Twos Complement Format

Temperature (°C)	Decimal	Hex	Binary
+105	+1002	0x3EA	0011 1110 1010
+85	+731	0x2DB	0010 1101 1011
+31.14771	+2	0x002	0000 0000 0010
+31.07386	+1	0x001	0000 0000 0001
+31	0	0x000	0000 0000 0000
+30.92614	−1	0xFFF	1111 1111 1111
+30.85229	−2	0xFFE	1111 1111 1110
−40	−962	0xC3E	1100 0011 1110

SYSTEM FUNCTIONS

GLOBAL COMMANDS

The GLOB_CMD register in Table 19 provides trigger bits for software reset, flash memory management, and calibration control. Start each of these functions by writing a 1 to the assigned bit in GLOB_CMD. After completing the task, the bit automatically returns to 0.

For example, set GLOB_CMD[7] = 1 (DIN = 0xBE80) to initiate a software reset. Set GLOB_CMD[3] = 1 (DIN = 0xBE08) to back up the user register contents in nonvolatile flash. This sequence includes loading the control registers with the data in their respective flash memory locations prior to producing new data.

Table 19. GLOB_CMD (Base Address = 0x3E), Write Only

Bits	Description (Default = 0x0000)
[15:8]	Not used
7	Software reset
[6:4]	Not used
3	Flash update
2	Not used
1	Factory calibration restore
0	Gyroscope bias correction

PRODUCT IDENTIFICATION

The PROD_ID register in Table 22 contains the binary equivalent of 16,445. It provides a product-specific variable for systems that need to track this in their system software. The LOT_ID1 and LOT_ID2 registers in Table 20 and Table 21, respectively, combine to provide a unique, 32-bit lot identification code.

The SERIAL_NUM register in Table 23 contains a binary number that represents the serial number on the device label. The assigned serial numbers in SERIAL_NUM are lot specific.

Table 20. LOT_ID1 (Base Address = 0x52), Read Only

Bits	Description
[15:0]	Lot identification, binary code

Table 21. LOT_ID2 (Base Address = 0x54), Read Only

Bits	Description
[15:0]	Lot identification, binary code

Table 22. PROD_ID (Base Address = 0x56), Read Only

Bits	Description (Default = 0x403D)
[15:0]	Product identification = 0x403D (16,445)

Table 23. SERIAL_NUM (Base Address = 0x58), Read Only

Bits	Description
[15:12]	Reserved
[11:0]	Serial number, 1 to 4094 (0xFFE)

SELF-TEST FUNCTION

The MSC_CTRL register in Table 24 provides a self-test function for the gyroscopes and accelerometers. This function allows the user to verify the mechanical integrity of each MEMS sensor. When enabled, the self test applies an electrostatic force to each internal sensor element, which causes them to move. The movement in each element simulates its response to actual rotation/acceleration and generates a predictable electrical response in the sensor outputs. Set MSC_CTRL[10] = 1 (DIN = 0xB504) to activate the internal self-test routine, which compares the response to an expected range of responses and reports a pass/fail response to DIAG_STAT[5]. If this bit is high, review DIAG_STAT[15:10] to identify the failing sensor.

Table 24. MSC_CTRL (Base Address = 0x34), Read/Write

Bits	Description (Default = 0x0006)
[15:12]	Not used
11	Checksum memory test (cleared upon completion)[1] 1 = enabled, 0 = disabled
10	Internal self test (cleared upon completion)[1] 1 = enabled, 0 = disabled
[9:8]	Do not use, always set to 00
7	Not used
6	Point of percussion, see Figure 21 1 = enabled, 0 = disabled
[5:3]	Not used
2	Data ready enable 1 = enabled, 0 = disabled
1	Data ready polarity 1 = active high when data is valid 0 = active low when data is valid
0	Data ready line select 1 = DIO2, 0 = DIO1

[1] The bit is automatically reset to 0 after finishing the test.

STATUS/ERROR FLAGS

The DIAG_STAT register in Table 25 provides error flags for a number of functions. Each flag uses 1 to indicate an error condition and 0 to indicate a normal condition. Reading this register provides access to the status of each flag and resets all of the bits to 0 for monitoring future operation. If the error condition remains, the error flag returns to 1 at the conclusion of the next sample cycle. DIAG_STAT[0] does not require a read of this register to return to 0. If the power supply voltage goes back into range, this flag clears automatically. The SPI communication error flag in DIAG_STAT[3] indicates that the number of SCLKs in a SPI sequence did not equal a multiple of 16 SCLKs.

Table 25. DIAG_STAT (Base Address = 0x3C), Read Only

Bits	Description (Default = 0x0000)
15	Z-axis accelerometer self-test failure 1 = fail, 0 = pass
14	Y-axis accelerometer self-test failure 1 = fail, 0 = pass
13	X-axis accelerometer self-test failure 1 = fail, 0 = pass
12	Z-axis gyroscope self-test failure 0 = pass
11	Y-axis gyroscope self-test failure 1 = fail, 0 = pass
10	X-axis gyroscope self-test failure 1 = fail, 0 = pass
9	Alarm 2 status 1 = active, 0 = inactive
8	Alarm 1 status 1 = active, 0 = inactive
7	Not used
6	Flash test, checksum flag 1 = fail, 0 = pass
5	Self-test diagnostic error flag 1 = fail, 0 = pass
4	Sensor overrange 1 = overrange, 0 = normal
3	SPI communication failure 1 = fail, 0 = pass
2	Flash update failure 1 = fail, 0 = pass
[1:0]	Not used

MEMORY MANAGEMENT

The FLASH_CNT register in Table 26 provides a 16-bit counter that helps track the number of write cycles to the nonvolatile flash memory. The flash updates every time a manual flash update occurs. A manual flash update is initiated by the GLOB_CMD[3] bit and is performed at the completion of the GLOB_CMD[1:0] functions (see Table 19).

Table 26. FLASH_CNT (Base Address = 0x00), Read Only

Bits	Description
[15:0]	Binary counter

Checksum Test

Set MSC_CTRL[11] = 1 (DIN = 0xB508) to perform a checksum test of the internal program memory. This function takes a summation of the internal program memory and compares it with the original summation value for the same locations (from factory configuration). If the sum matches the correct value, DIAG_STAT[6] is equal to 0. If it does not match, DIAG_STAT[6] is equal to 1. Make sure that the power supply is within specification for the entire 20 ms that this function takes to complete.

INPUT/OUTPUT CONFIGURATION

DATA READY INDICATOR

The data ready indicator provides a signal that indicates when the registers are updating, so that system processors can avoid data collision, a condition when internal register updates happen at the same time that an external processor requests it. The data ready signal has valid and invalid states. Using the transition from invalid to valid to trigger an interrupt service routine provides the most time for data acquisition (before the next register update). See Figure 4 and Table 2 for specific timing information.

MSC_CTRL[2:0] (see Table 24) provide control bits for enabling this function, selecting the polarity of the valid state and I/O line assignment (DIO1, DIO2). The factory default setting of MSC_CTRL[2:0] = 110 establishes DIO1 as a data ready output line and assigns the valid state with a logic high (1). Set MSC_CTRL[2:0] = 100 (DIN = 0xB404) to change the polarity of the data ready signal on DIO1 for interrupt inputs that require negative logic inputs for activation.

GENERAL-PURPOSE INPUT/OUTPUT

DIO1, DIO2, DIO3, and DIO4 are configurable, general-purpose input/output lines that serve multiple purposes. The data ready controls in MSC_CTRL[2:0] have the highest priority for configuring DIO1 and DIO2. The alarm indicator controls in ALM_CTRL[2:0] have the second highest priority for configuring DIO1 and DIO2. The external clock control associated with SMPL_PRD[0] has the highest priority for DIO4 configuration (see Table 28). GPIO_CTRL in Table 27 has the lowest priority for configuring DIO1, DIO2, and DIO4, and has absolute control over DIO3.

Table 27. GPIO_CTRL (Base Address = 0x32), Read/Write

Bits	Description (Default = 0x0000)
[15:12]	Not used
11	General-Purpose I/O Line 4 (DIO4) data level
10	General-Purpose I/O Line 3 (DIO3) data level
9	General-Purpose I/O Line 2 (DIO2) data level
8	General-Purpose I/O Line 1 (DIO1) data level
[7:4]	Not used
3	General-Purpose I/O Line 4 (DIO4) direction control 1 = output, 0 = input
2	General-Purpose I/O Line 3 (DIO3) direction control 1 = output, 0 = input
1	General-Purpose I/O Line 2 (DIO2) direction control 1 = output, 0 = input
0	General-Purpose I/O Line 1 (DIO1) direction control 1 = output, 0 = input

Example Input/Output Configuration

For example, set GPIO_CTRL[3:0] = 0100 (DIN = 0xB204) to set DIO3 as an output signal pin and DIO1, DIO2, and DIO4 as input signal pins. Set the output on DIO3 to 1 by setting GPIO_CTRL[10] = 1 (DIN = 0xB304). Then, read GPIO_CTRL[7:0] (DIN = 0x3200) and mask off GPIO_CTRL[9:8] and GPIO_CTRL[11] to monitor the digital signal levels on DIO4, DIO2, and DIO1.

DIGITAL PROCESSING CONFIGURATION

GYROSCOPES/ACCELEROMETERS

Figure 19 provides a diagram that describes all signal processing components for the gyroscopes and accelerometers. The internal sampling system produces new data in the xGYRO_OUT and xACCL_OUT output data registers at a rate of 819.2 SPS. The SMPL_PRD register in Table 28 provides two functional controls that affect sampling and register update rates. SMPL_PRD[12:8] provides a control for reducing the update rate, using an averaging filter with a decimated output. These bits provide a binomial control that divides the data rate by a factor of 2 every time this number increases by 1. For example, set SMPL_PRD[15:8] = 0x04 (DIN = 0xB704) to set the decimation factor to 16. This reduces the update rate to 51.2 SPS and the bandwidth to ~25 Hz. The SMPL_PRD[12:8] setting affects the update rate for the TEMP_OUT register (see Table 17) as well.

Table 28. SMPL_PRD (Base Address = 0x36), Read/Write

Bits	Description (Default = 0x0001)
[15:13]	Not used
[12:8]	D, decimation rate setting, binomial, see Figure 19
[7:1]	Not used
0	Clock 1 = internal sampling clock, 819.2 SPS 0 = external sampling clock

INPUT CLOCK CONFIGURATION

SMPL_PRD[0] (see Table 28) provides a control for synchronizing the internal sampling to an external clock source. Set SMPL_PRD[0] = 0 (DIN = 0xB600) and GPIO_CTRL[3] = 0 (DIN = 0xB200) to enable the external clock. See Table 2 and Figure 4 for timing information.

Digital Filtering

The SENS_AVG register in Table 29 provides user controls for the low-pass filter. This filter contains two cascaded averaging filters that provide a Bartlett window, FIR filter response (see Figure 19). For example, set SENS_AVG[2:0] = 100 (DIN = 0xB804) to set each stage to 16 taps. When used with the default sample rate of 819.2 SPS and zero decimation (SMPL_PRD[15:8] = 0x00), this value reduces the sensor bandwidth to approximately 16 Hz.

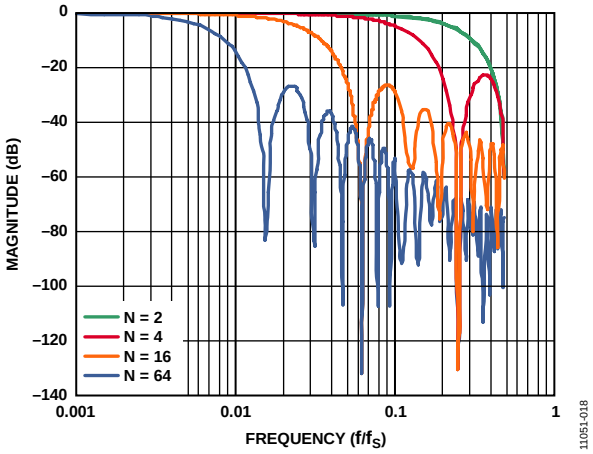


Figure 18. Bartlett Window, FIR Filter Frequency Response (Phase Delay = N Samples)

Dynamic Range

The SENS_AVG[10:8] bits provide three dynamic range settings for the gyroscopes. The lower dynamic range settings (±62.5°/sec and ±125°/sec) limit the minimum filter tap sizes to maintain resolution. For example, set SENS_AVG[10:8] = 010 (DIN = 0xB902) for a measurement range of ±125°/sec. Because this setting can influence the filter settings, program SENS_AVG[10:8] before programming SENS_AVG[2:0] if more filtering is required.

Table 29. SENS_AVG (Base Address = 0x38), Read/Write

Bits	Description (Default = 0x0402)
[15:11]	Not used
[10:8]	Measurement range (sensitivity) selection 100 = ±250°/sec (default condition) 010 = ±125°/sec, filter taps ≥ 4 (Bits[2:0] ≥ 0x02) 001 = ±62.5°/sec, filter taps ≥ 16 (Bits[2:0] ≥ 0x04)
[7:3]	Not used
[2:0]	Filter Size Variable B Number of taps in each stage; $N_B = 2^B$ See Figure 18 for filter response

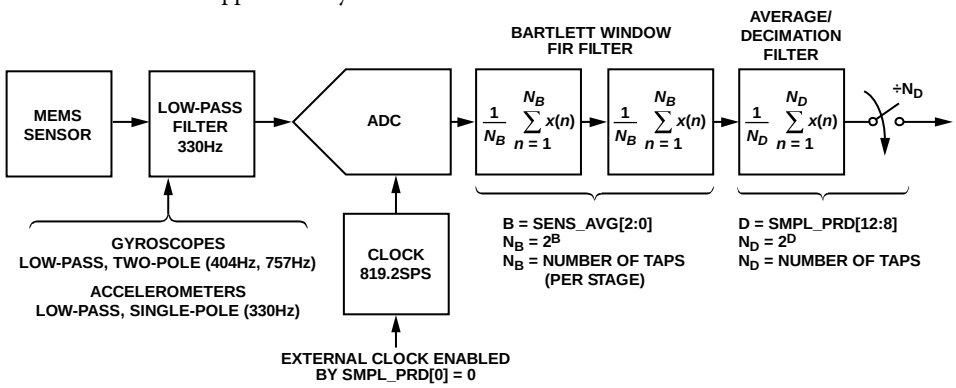


Figure 19. Sampling and Frequency Response Block Diagram

CALIBRATION

The mechanical structure and assembly process of the ADIS16445 provide excellent position and alignment stability for each sensor, even after subjected to temperature cycles, shock, vibration, and other environmental conditions. The factory calibration includes a dynamic characterization of each gyroscope and accelerometer over temperature and generates sensor specific correction formulas.

GYROSCOPES

The XGYRO_OFF (see Table 30), YGYRO_OFF (see Table 31), and ZGYRO_OFF (see Table 32) registers provide user-programmable bias adjustment function for the x-, y-, and z-axis gyroscopes, respectively. Figure 20 illustrates that they contain bias correction factors that adjust to the sensor data immediately before it loads into the output register.

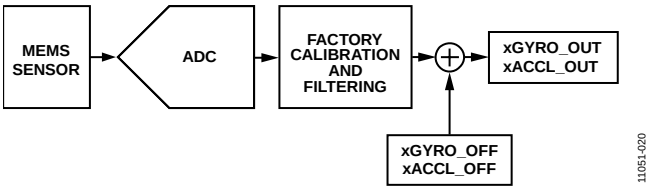


Figure 20. User Calibration, Gyroscopes, and Accelerometers

Gyroscope Bias Error Estimation

Any system level calibration function must start with an estimate of the bias errors, which typically comes from a sample of gyroscope output data, when the device is not in motion. The sample size of data depends on the accuracy goals. Figure 7 provides a trade-off relationship between averaging time and the expected accuracy of a bias measurement. Vibration, thermal gradients, and power supply instability can influence the accuracy of this process.

Table 30. XGYRO_OFF (Base Address = 0x1A), Read/Write

Bits	Description (Default = 0x0000)
[15:0]	X-axis, gyroscope offset correction factor, twos complement, 0.0025°/sec/LSB, 0°/sec = 0x0000

Table 31. YGYRO_OFF (Base Address = 0x1C), Read/Write

Bits	Description (Default = 0x0000)
[15:0]	Y-axis, gyroscope offset correction factor, twos complement, 0.0025°/sec/LSB, 0°/sec = 0x0000

Table 32. ZGYRO_OFF (Base Address = 0x1E), Read/Write

Bits	Description (Default = 0x0000)
[15:0]	Z-axis, gyroscope offset correction factor, twos complement, 0.0025°/sec/LSB, 0°/sec = 0x0000

Gyroscope Bias Correction Factors

When the bias estimate is complete, multiply the estimate by −1 to change its polarity, convert it into digital format for the offset correction registers (see Table 30, Table 31, and Table 32), and write the correction factors to the correction registers. For example, lower the x-axis bias by 10 LSB (0.025°/sec) by setting XGYRO_OFF = 0x1FF6 (DIN = 0x9B1F, 0x9AF6).

Single Command Bias Correction

GLOB_CMD[0] (see Table 19) loads the xGYRO_OFF registers with the values that are the opposite of the values that are in xGYRO_OUT, at the time of initiation. Use this command, together with the decimation filter (SMPL_PRD[12:8], see Table 28), to automatically average the gyroscope data and improve the accuracy of this function, as follows:

1. Set SENS_AVG[10:8] = 001 (DIN = 0xB901) to optimize the xGYRO_OUT sensitivity to 0.0025 °/sec/LSB.
2. Set SMPL_PRD[12:8] = 0x10 (DIN = 0xB710) to set the decimation rate to 65,536 (2^{16}), which provides an averaging time of 80 seconds (65,536 ÷ 819.2 SPS).
3. Wait for 80 seconds while keeping the device motionless.
4. Set GLOB_CMD[0] = 1 (DIN = 0xBE01) and wait for the time it takes to perform the flash memory backup.

ACCELEROMETERS

The XACCL_OFF (see Table 33), YACCL_OFF (see Table 34), and ZACCL_OFF (see Table 35) registers provide user programmable bias adjustment function for the x-, y-, and z-axis accelerometers, respectively. These registers adjust the accelerometer data in the same manner as XGYRO_OFF in Figure 20.

Table 33. XACCL_OFF (Base Address = 0x20), Read/Write

Bits	Description (Default = 0x0000)
[15:0]	X-axis, accelerometer offset correction factor, twos complement, 0.25 m*g*/LSB, 0 *g* = 0x0000

Table 34. YACCL_OFF (Base Address = 0x22), Read/Write

Bits	Description (Default = 0x0000)
[15:14]	Not used
[13:0]	Y-axis, accelerometer offset correction factor, twos complement, 0.25 m*g*/LSB, 0 *g* = 0x0000

Table 35. ZACCL_OFF (Base Address = 0x24), Read/Write

Bits	Description (Default = 0x0000)
[15:14]	Not used
[13:0]	Z-axis, accelerometer offset correction factor, twos complement, 0.25 m*g*/LSB, 0 *g* = 0x0000

Accelerometer Bias Error Estimation

Under static conditions, orient each accelerometer in positions where the response to gravity is predictable. A common approach is to measure the response of each accelerometer when they are oriented in peak response positions, that is, where ±1 *g* is the ideal measurement position. Next, average the +1 *g* and −1 *g* accelerometer measurements together to estimate the residual bias error. Using more points in the rotation can improve the accuracy of the response.

Accelerometer Bias Correction Factors

When the bias estimate is complete, multiply the estimate by −1 to change its polarity, convert it to the digital format for the offset correction registers (see Table 33, Table 34 or Table 35), and write the correction factors to the correction registers. For example, lower the x-axis bias by 12 LSB (3 m*g*) by setting XACCL_OFF = 0xFFF4 (DIN = 0xA1FF, 0xA0F4).

Point of Percussion Alignment

Set MSC_CTRL[6] = 1 (DIN = 0xB446) to enable this feature and maintain the factory default settings for DIO1. This feature performs a point of percussion translation to the point identified in Figure 21. See Table 24 for more information on MSC_CTRL.

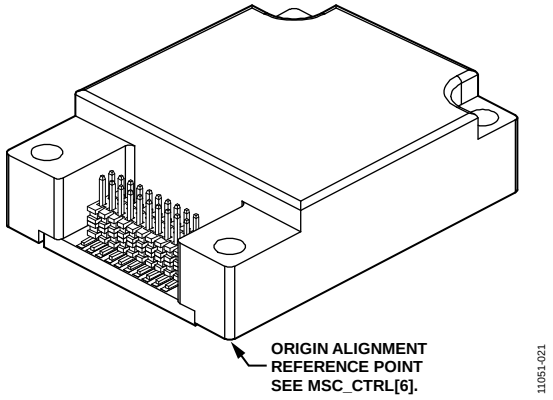


Figure 21. Point of Percussion Physical Reference

FLASH UPDATES

When using the user calibration registers to optimize system level accuracy, set GLOB_CMD[3] = 1 (DIN = 0xBE04) to save these settings in nonvolatile flash memory. Be sure to consider the endurance rating of the flash memory when determining how often to update the user correction factors in the flash memory.

RESTORING FACTORY CALIBRATION

Set GLOB_CMD[1] = 1 (DIN = 0xBE02) to execute the factory calibration restore function, which resets the gyroscope and accelerometer offset registers to 0x0000 and all sensor data to 0. Then, it automatically updates the flash memory and restarts sampling and processing data. See Table 19 for information on GLOB_CMD.

ALARMS

Alarm 1 and Alarm 2 provide two independent alarms with programmable levels, polarity, and data sources.

STATIC ALARM USE

The static alarms setting compares the data source selection (ALM_CTRL[15:8]) with the values in the ALM_MAGx registers listed in Table 36 and Table 37, using ALM_MAGx[15] to determine the trigger polarity. The data format in these registers matches the format of the data selection in ALM_CTRL[15:8]. See Table 41, Alarm 1, for a static alarm configuration example.

Table 36. ALM_MAG1 (Base Address = 0x40), Read/Write

Bits	Description (Default = 0x0000)
[15:0]	Threshold setting; matches for format of ALM_CTRL[11:8] output register selection

Table 37. ALM_MAG2 (Base Address = 0x42), Read/Write

Bits	Description (Default = 0x0000)
[15:0]	Threshold setting; matches for format of ALM_CTRL[15:12] output register selection

DYNAMIC ALARM USE

The dynamic alarm setting monitors the data selection for a rate-of-change comparison. The rate-of-change comparison is represented by the magnitude in the ALM_MAGx registers over the time represented by the number-of-samples setting in the ALM_SMPLx registers, located in Table 38 and Table 39. See Table 41, Alarm 2, for a dynamic alarm configuration example.

Table 38. ALM_SMPL1 (Base Address = 0x44), Read/Write

Bits	Description (Default = 0x0000)
[15:8]	Not used
[7:0]	Binary, number of samples (both 0x00 and 0x01 = 1)

Table 39. ALM_SMPL2 (Base Address = 0x46), Read/Write

Bits	Description (Default = 0x0000)
[15:8]	Not used
[7:0]	Binary, number of samples (both 0x00 and 0x01 = 1)

ALARM REPORTING

The DIAG_STAT[9:8] bits provide error flags that indicate an alarm condition. The ALM_CTRL[2:0] bits provide controls for a hardware indicator using DIO1 or DIO2.

Table 40. ALM_CTRL (Base Address = 0x48), Read/Write

Bits	Description (Default = 0x0000)
[15:12]	Alarm 2 data source selection 0000 = disable 0001 = XGYRO_OUT 0010 = YGYRO_OUT 0011 = ZGYRO_OUT 0100 = XACCL_OUT 0101 = YACCL_OUT 0110 = ZACCL_OUT
[11:8]	Alarm 1 data source selection (same as Alarm 2)
7	Alarm 2, dynamic/static (1 = dynamic, 0 = static)
6	Alarm 1, dynamic/static (1 = dynamic, 0 = static)
5	Alarm 2, polarity (1 = greater than ALM_MAG2)
4	Alarm 1, polarity (1 = greater than ALM_MAG1)
3	Data source filtering (1 = filtered, 0 = unfiltered)
2	Alarm indicator (1 = enabled, 0 = disabled)
1	Alarm indicator active polarity (1 = high, 0 = low)
0	Alarm output line select (1 = DIO2, 0 = DIO1)

Alarm Example

Table 41 offers an example that configures Alarm 1 to trigger when filtered ZACCL_OUT data drops below 0.7 *g*, and Alarm 2 to trigger when filtered ZGYRO_OUT data changes by more than 50 °/sec over a 100 ms period, or 500 °/sec^2. The filter setting helps reduce false triggers from noise and refines the accuracy of the trigger points. The ALM_SMPL2 setting of 82 samples provides a comparison period that is approximately equal to 100 ms for an internal sample rate of 819.2 SPS.

Table 41. Alarm Configuration Example

DIN	Description
0xCD36, 0xCCAF	ALM_CTRL = 0x36AF Alarm 2: dynamic, Δ-ZGYRO_OUT (Δ-time, ALM_SMPL2) > ALM_MAG2 Alarm 1: static, ZACCL_OUT < ALM_MAG1, filtered data DIO2 output indicator, positive polarity
0xC713, 0xC688	ALM_MAG2 = 0x1388 = 5000 LSB = 50 °/sec
0xC50A, 0xC4F0	ALM_MAG1 = 0x0AF0 = 2800 LSB = +0.7 *g*
0xC866	ALM_SMPL2[7:0] = 0x52 = 82 samples 82 samples ÷ 819.2 SPS = ~100 ms

APPLICATIONS INFORMATION

POWER SUPPLY CONSIDERATIONS

The power supply must be within 3.15 V and 3.45 V for normal operation and optimal performance. During start up, the internal power conversion system starts drawing current when VDD reaches 1.6 V. The internal processor begins initializing when VDD is equal to 2.35 V. After the processor starts, VDD must reach 2.7 V within 128 ms. Also, make sure that the power supply drops below 1.6 V to shut the device down. Figure 9 shows a 10 µF capacitor on the power supply. Using this capacitor supports optimal noise performance in the sensors.

ADIS16445/PCBZ

The ADIS16445/PCBZ includes one ADIS16445AMLZ, one interface PCB, and one flexible connector/cable. This particular flexible cable mates the ADIS16445AMLZ to any system that is currently using the ADIS1636x, ADIS16375, ADIS16385, ADIS1640x, or ADIS1648x IMU products, which use a 24-pin interface, rather than the 20-pin interface that the ADIS16445 uses. This combination of components enables quicker installation for prototype evaluation and algorithm development. Figure 22 provides a mechanical design example for using these three components in a system.

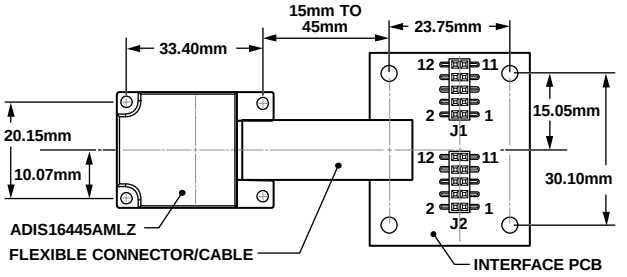


Figure 22. Physical Diagram for Mounting the ADIS16445/PCBZ

Figure 23 provides the pin assignments for the interface board.

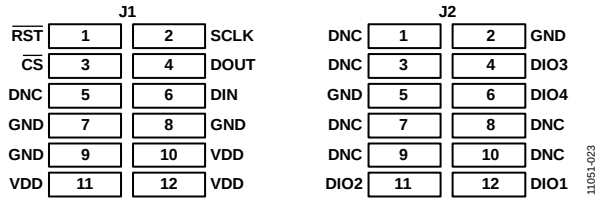


Figure 23. J1/J2 Pin Assignments for Interface PCB

Installation

The following steps provide an example installation process for using these three components:

- Drill and tap M2 and M3 holes in the system frame, according to the locations in Figure 22.
- Install the ADIS16445 using M2 machine screws. Use a mounting torque of 25 inch-ounces.
- Install the interface PCB using M3 machine screws.
- Connect J1 on the interface flex to the ADIS16445AMLZ connector.
- Connect J2 on the interface flex to J3 on the interface PCB. Note that J2 (interface flex) has 20 pins and J3 (interface PCB) has 24 pins. Make sure that Pin 1 on J2 (interface flex) connects to Pin 20 on J3 (interface PCB). J3 has a Pin 1 indicator to help guide this connection.
- Use J1 and J2 on the interface PCB to make the electrical connection with the system supply and embedded processor, using 12-pin, 1 mm ribbon cables. The following parts may be useful in building this type of cable: 3M Part Number 152212-0100-GB (ribbon crimp connector) and 3M Part Number 3625/12 (ribbon cable).

The C1/C2 pads on the interface PCB do not have capacitors on them, but these pads can support the suggested power supply capacitor of 10 µF (see Figure 9).

PC-BASED EVALUATION TOOLS

The EVAL-ADIS supports PC-based evaluation of the ADIS16445. Go to www.analog.com/EVAL-ADIS, to download the user guide (UG-287) and software (IMU evaluation).

MOUNTING APPROACHES

Mounting, Connector Up

The ADIS16445 supports both connector-up and connector-down mounting approaches. Figure 24 offers an example of a connector-up mounting approach, which uses a flexible interface cable for the electrical connection. The connector-up approach provides a simple mechanical design, but requires the use of a flexible connector. When connecting to legacy systems that use other Analog Devices IMU products (ADIS163xx/ADIS164xx), the connector-up method may be the simplest approach for migrating to the ADIS16445. Figure 22 provide an example for the mechanical design that uses a connector-up mounting approach.

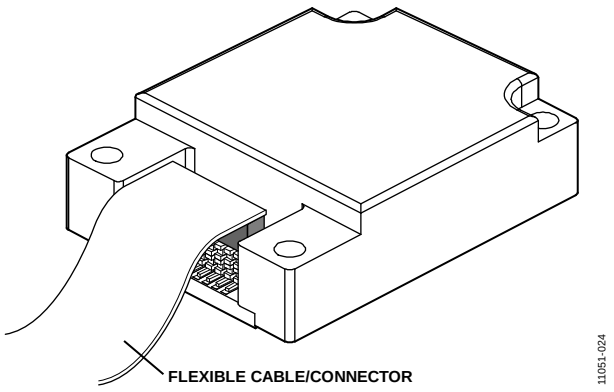


Figure 24. Connector-Up Mounting Example

Mounting, Connector Down

The connector-down approach requires a little more complexity in the PCB design, but eliminates the need for the flexible connector. The bottom side of the ADIS16445AMLZ package accommodates M2 machine screws that have a head diameter of 3.5 mm and a countersink angle of 45°.

Figure 25 provides a graphical example of a connector-down mounting approach. This example uses countersunk M2 × 0.4 mm × 12 mm machine screws to secure the ADIS16445AMLZ to a bulkhead, which is below the PCB that contains the mating connector. Figure 26 provides a design example for this PCB.

When finalizing this design for a particular PCB vendor, follow the vendor design rules to make sure that the top of the ADIS16445AMLZ package slides through the cutout after PCB fabrication. When using the alignment holes associated with the mating connector (CLM-110-02-LM-D-A, Samtec) and M2 machine screws for the mounting hardware, the 2.4 mm mounting hole diameter provides sufficient flexibility to account for tolerance in connector location (on both the ADIS16445AMLZ and in the mating PCB). For more information and design tools, visit the Package and Resources section available at www.analog.com/ADIS16445.

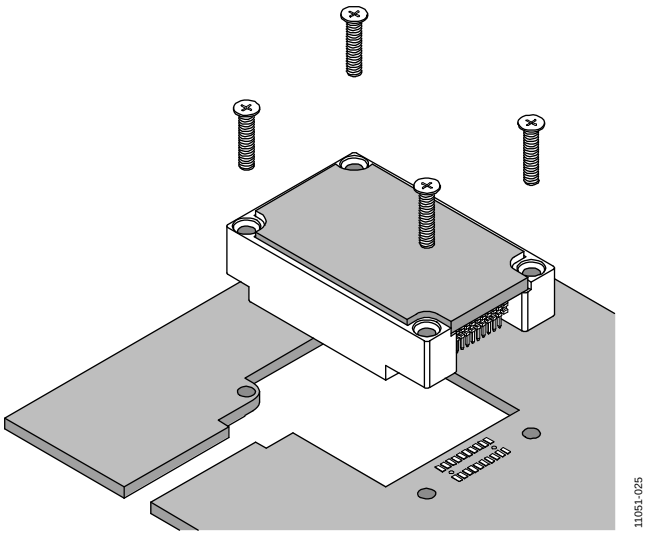


Figure 25. Connector-Down Mounting Example

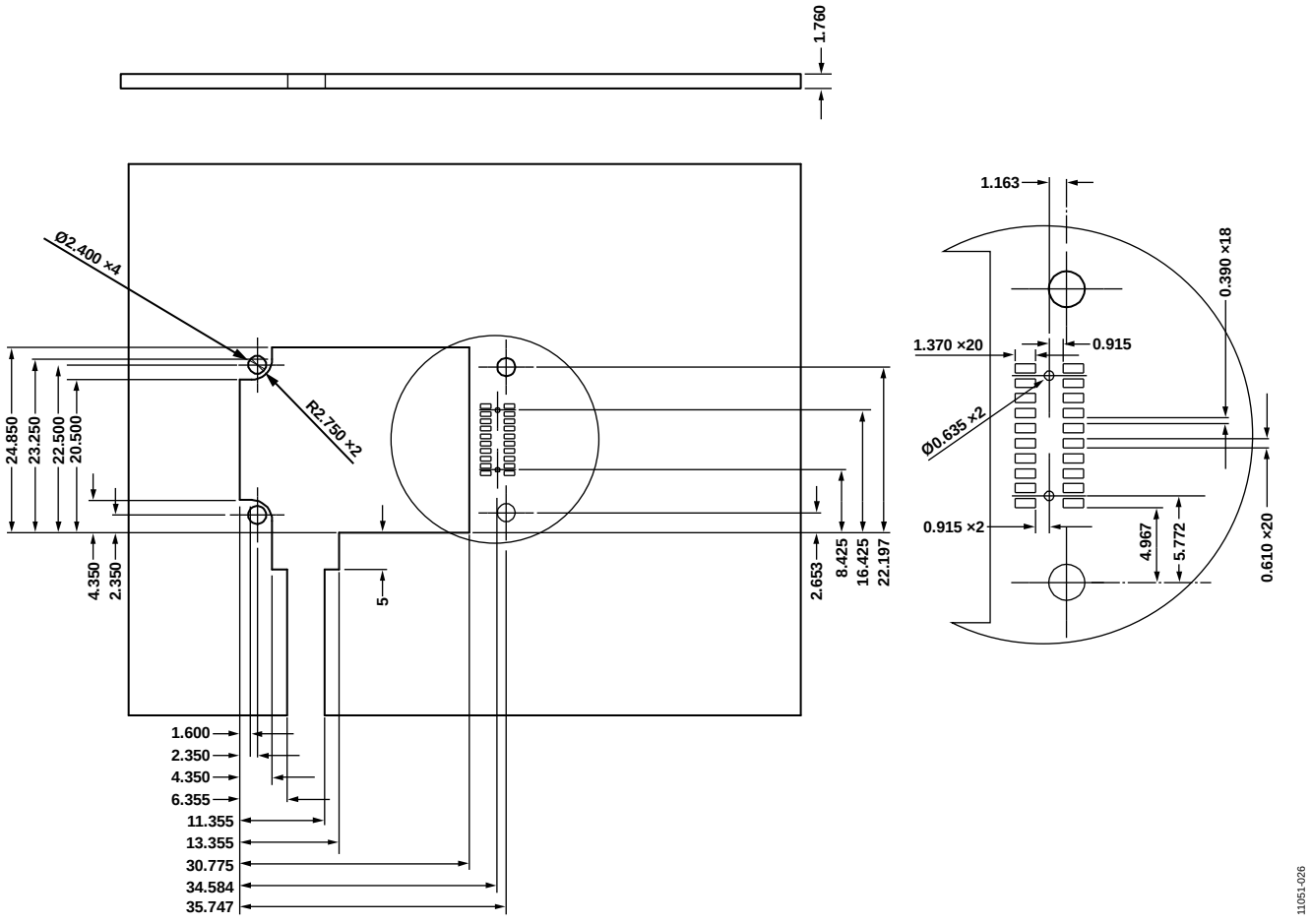


Figure 26. Connector-Down PCB Design Example

OUTLINE DIMENSIONS

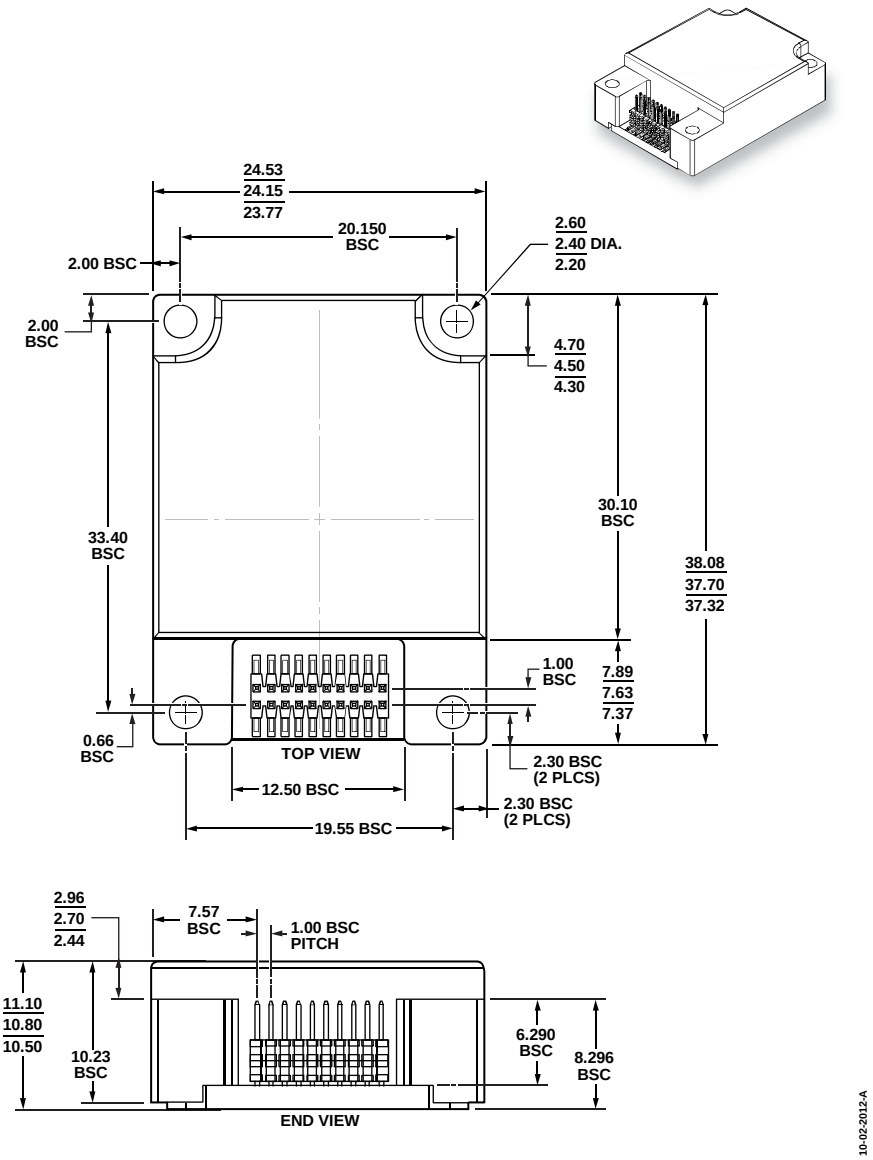


Figure 27. 20-Lead Module with Connector Interface [MODULE]
(ML-20-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADIS16445AMLZ	−40°C to +85°C	20-Lead Module with Connector Interface [MODULE]	ML-20-3
ADIS16445/PCBZ		Interface PCB	

[1] Z = RoHS Compliant Part.

NOTES

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